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# Proximity effects of beryllium-doped GaN buffer layers on the electronic properties of epitaxial AlGaN/GaN heterostructures

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ABSTRACT

AlGaN/GaN/Be:GaN heterostructures have been grown by rf-plasma molecular beam epitaxy on free-standing semi-insulating GaN substrates, employing unintentionally-doped (UID) GaN buffer layers with thicknesses, $d_{UID}$, varying between 50 nm and 500 nm. We have found that the heterostructures with UID buffers thicker than 200 nm exhibit much improved Hall properties and inter-device isolation current compared to heterostructures with $d_{UID} < 200$ nm. The output conductance of devices fabricated on these heterostructures increases as $d_{UID}$ decreases below 200 nm, and devices with gate lengths of 240 nm and 1 μm exhibited no significant difference in output conductance. Evidence of buffer trapping is observed in devices for which $d_{UID} \leqslant 100$ nm. The observed effects are tentatively explained by the presence of parallel conduction paths in samples with non-optimized UID buffer thickness.

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## 1. Introduction

Significant improvements have been made recently in the performance of AlGaN/GaN high electron mobility transistors (HEMTs) devices grown by a variety of techniques and on a variety of substrates [1–4]. The increasing availability in recent years of free-standing, hydride vapor phase epitaxy (HVPE) grown GaN substrates has enabled the growth by molecular beam epitaxy (MBE) of AlGaN/GaN HEMTs with significantly lower threading dislocation densities and correspondingly higher crystal quality than similar devices on non-native substrates [5,6]. However, secondary ion mass spectroscopy (SIMS) analysis of rf-plasma assisted MBE-grown homoepitaxial GaN has shown that oxygen, a shallow donor in GaN, is present at the regrowth interface in concentrations in excess of $10^{19}$ cm$^{-3}$ and persists in the epitaxial layer in diminishing concentrations within an interface region of ~500 nm [7]. Beyond this interface region the background concentration of oxygen ranges from ~$10^{17}$ cm$^{-3}$ to the SIMS detection limit, ~$2 \times 10^{16}$ cm$^{-3}$. Combined with a low density of acceptor-like threading dislocations, the presence of oxygen leads to conductivity of the unintentionally-doped (UID) homoepitaxial GaN which is undesirable for microwave device applications and must be remedied, for instance, by using a compensating acceptor such as beryllium [5,6,8,9]. Alternative approaches employing carbon [10,11] or iron [12–14] have been used to similar effect in GaN buffers grown on non-native substrates. Recent studies suggest that compensation-doped GaN layers may have modestly deleterious effects on the dc or microwave properties of AlGaN/GaN HEMTs grown on SiC substrates [11,15], and that these effects may vary with the proximity of the doped layer to the two-dimensional electron gas (2DEG). The aim of the present work is to investigate this proximity effect of beryllium-doped GaN layers on the electronic properties of AlGaN/GaN HEMTs grown by rf-MBE on native GaN substrates.

## 2. Experimental

Seven AlGaN/GaN heterostructures were grown by rf-plasma assisted MBE on free-standing, semi-insulating (SI) GaN substrates. The substrates were grown by HVPE and were doped with iron at a nominal concentration of $10^{18}$ cm$^{-3}$. Contactless resistance measurements on similar wafers indicate a bulk resistivity in excess of $10^9$ Ω cm. All sample growths were performed on the Ga-polar, *c*-plane surfaces of the free-standing wafers. These surfaces were chemical–mechanically polished. Prior to loading into the ultra-high vacuum (UHV) MBE system the substrates were degreased with organic solvents and etched with acid and base solutions.

Each of the heterostructures consisted of a 250-Å $Al_xGa_{1-x}N$ barrier ($x = 0.28$), an unintentionally-doped GaN buffer, and a $10^{19}$ cm$^{-3}$ beryllium-doped GaN layer as described in Table 1.

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14. ABSTRACT

**AlGaN/GaN/Be:GaN heterostructures have been grown by rf-plasma molecular beam epitaxy on freestanding semi-insulating GaN substrates, employing unintentionally-doped (UID) GaN buffer layers with thicknesses, dUID, varying between 50 nm and 500 nm. We have found that the heterostructures with UID buffers thicker than 200 nm exhibit much improved Hall properties and inter-device isolation current compared to heterostructures with dUID < 200 nm. The output conductance of devices fabricated on these heterostructures increases as dUID decreases below 200 nm, and devices with gate lengths of 240 nm and 1 lmexhibited no significant difference in output conductance. Evidence of buffer trapping is observed in devices for which dUID 6 100 nm. The observed effects are tentatively explained by the presence of parallel conduction paths in samples with non-optimized UID buffer thickness.**

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Samples A–D were each grown with a 1-μm-thick Be-doped GaN buffer layer thickness, $d_{Be}$, and a variable UID layer thickness, $d_{UID}$, and therefore variable overall thickness. Samples E–G were grown with variable $d_{UID}$ but a constant overall heterostructure thickness of 1.5 μm (exclusive of the 250-Å AlGaN barrier). The final Sample ("G") was grown with a 450-nm "sub-buffer" between the HVPE GaN substrate and the 1-μm Be-doped layer in order to determine what effect, if any, was caused by displacing the doped layer away from the substrate. All epitaxial layer growths proceeded at elemental (Al, Ga, N) fluxes and at a substrate temperature (650 °C) which have yielded samples with consistently excellent structural and electrical properties [8,9]. The nominal beryllium concentration in all doped layers is $10^{19}$ cm$^{-3}$. We have previously demonstrated that beryllium concentrations up to $3 \times 10^{19}$ do not degrade the crystal quality of homoepitaxial GaN layers [16]. The GaN growth rate was measured on similar samples to be ~1 Å/s. Further details of substrate preparation and epitaxial growth can be found elsewhere [8,9].

Process control monitors, including circular transmission line measurement (CTLM), Hall/van der Pauw, and inter-device isolation test patterns, were fabricated using conventional contact lithography and liftoff. Ohmic contacts were formed using a Ti/Al/Ni/Au metal stack annealed at 900 °C for 30 s. Mesa isolation was accomplished using a 500-Å $BCl_3/Cl_2/Ar$ inductively coupled plasma (ICP) dry etch. On Samples A–D and F, gates were defined by e-beam lithography on devices with source-drain spacing, $L_{DS}$, of 3 μm and 5 μm. The gate lengths, $L_G$, were subsequently measured by scanning electron microscopy; Samples A–C and F had $L_G$ between 220 nm and 240 nm, while Sample D had $L_G$ = 400 nm, as shown in Table 1. On the remaining two Samples, E and G, gates with $L_G$ = 1 μm were defined by contact lithography and liftoff on devices with nominal $L_{DS}$ = 5 μm. The gate widths of all devices were 150 μm.

## 3. Results and discussion

Sheet resistance, $R_{sh}$, Hall mobility, $\mu$, and sheet density, $n_{sh}$, were measured on each sample. $R_{sh}$ measured by CTLM was consistent with the Hall sheet resistance measurements. Hall mobility, $\mu$, increased monotonically from ~1350 cm$^2$/V s to ~1660 cm$^2$/V s as $d_{UID}$ increased from 50 nm to 500 nm, with a sharp increase in $\mu$ occurring for $d_{UID}$ < 200 nm (Fig. 1). The Hall sheet density, $n_{sh}$, varied between 0.9 and 1.0 × $10^{13}$ cm$^{-2}$. For $d_{UID}$ < 200 nm $n_{sh}$ tended to increase as the UID layer thickness increased, and appeared to saturate at greater thicknesses within experimental errors, as shown in Fig. 2. We believe that the trend toward lower sheet density with thinner $d_{UID}$ is a result of partial depletion of the 2DEG by the Be-doped layer. The mechanism governing the dependence of mobility on $d_{UID}$ is still under investigation, though we believe the observed behavior is inconsistent with remote ionized impurity scattering from the doped layer. Further, SIMS analysis of similar samples indicates that the Be concentration diminishes between the doped and UID layer more rapidly than one decade per 25 nm, suggesting that impurity scattering from Be atoms which have diffused to the 2DEG is also unlikely.

**Table 1**
Sample ID, thicknesses of the unintentionally-doped GaN buffer ($d_{UID}$), Be-doped GaN isolation layer ($d_{Be}$), and unintentionally-doped sub-buffer ($d_{SB}$). Gate lengths of devices on these samples are indicated in the final column.

| Sample ID | $d_{UID}$ (nm) | $d_{Be}$ (nm) | $d_{SB}$ (nm) | $L_G$ (nm) |
|---|---|---|---|---|
| A | 50 | 1000 | 0 | 240 |
| B | 100 | 1000 | 0 | 220 |
| C | 200 | 1000 | 0 | 230 |
| D | 500 | 1000 | 0 | 400 |
| E | 50 | 1450 | 0 | 1000 |
| F | 100 | 1400 | 0 | 230 |
| G | 50 | 1000 | 450 | 1000 |

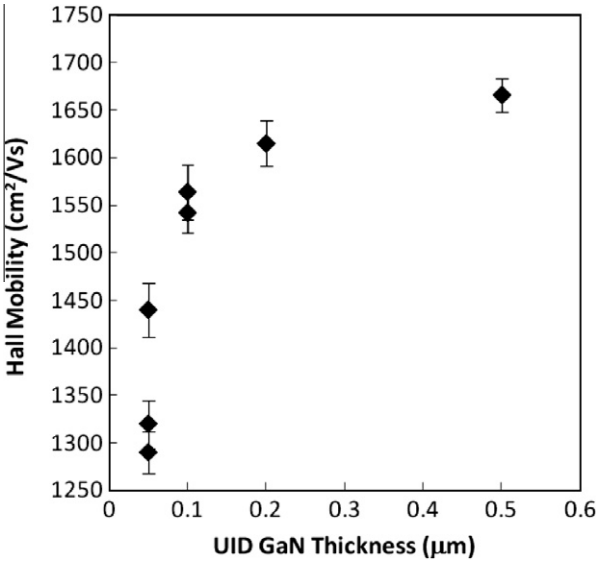


**Fig. 1.** Hall mobility versus UID GaN buffer thickness. Symbols indicate average measurements and error bars indicate the magnitude of the standard deviations on each sample.

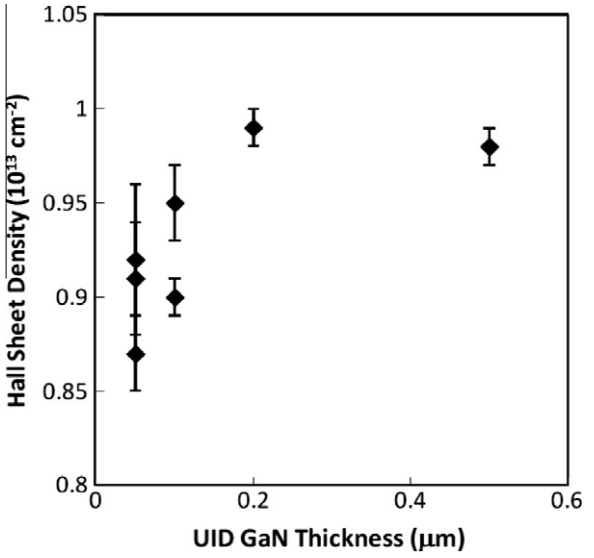


**Fig. 2.** 2DEG sheet density versus UID GaN buffer thickness. Symbols indicate average measurements and error bars indicate the magnitude of the standard deviations on each sample.

We observed significant differences between drain characteristic curves of the various samples. Two representative sets of curves from Samples A and C are shown in Fig. 3, denoted by closed and open symbols, respectively. The lower drain current densities of Sample A compared to that of Sample C at identical bias conditions are expected on the basis of higher sheet resistances observed at thinner $d_{UID}$. The visibly larger output conductance of Sample A is a common feature of devices on this sample. We have determined the output conductance of all devices as $g_D = (dI_D/dV_{DS})$ at $V_{GS} = -3$ V, $V_{DS} = 10$ V and the results are shown in Fig. 4. One can see a significant increase in $g_D$ as $d_{UID}$ decreases below 200 nm. In contrast, the output conductance of devices with buffer

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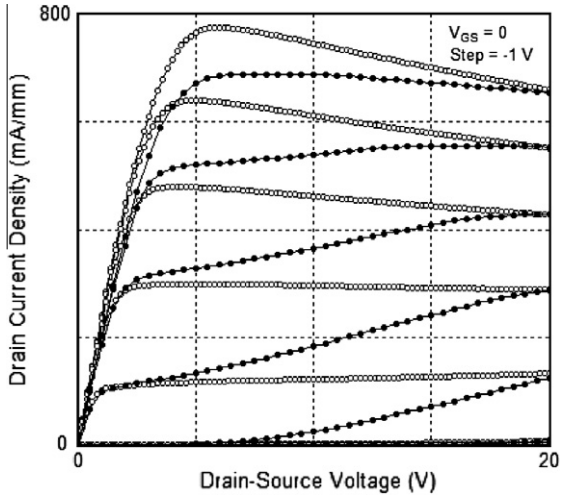


**Fig. 3.** Representative drain characteristics of HEMTs on Sample A (closed symbols, $d_{UID}$ = 50 nm) and Sample C (open symbols, $d_{UID}$ = 200 nm). The initial gate – source potential was 0 V and the step was −1 V. Note the larger output conductance visible in the drain curves of Sample A.

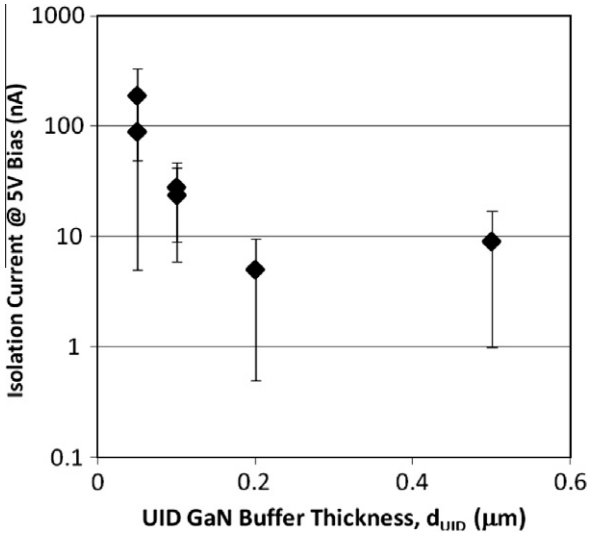


**Fig. 5.** Inter-device isolation current versus $d_{UID}$. Isolation currents were measured at 5 V bias across concentric ohmic contacts separated by a 16-μm annulus in which the 2DEG had been removed. The diameter of the inner contact was 100 μm.

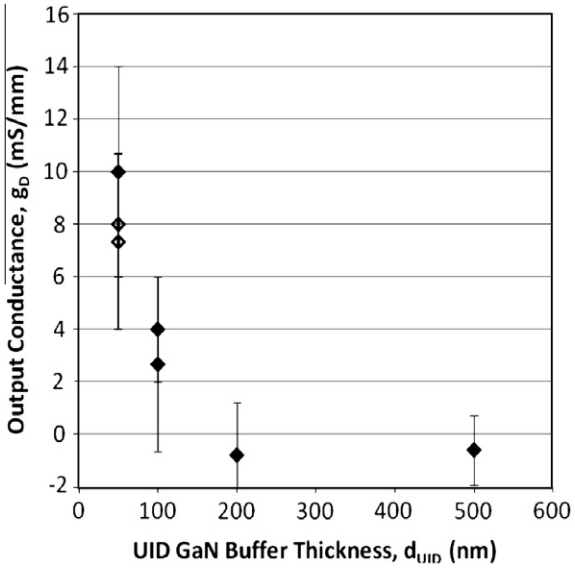


**Fig. 4.** Output conductance versus UID GaN buffer thickness. Output conductance was determined from the drain characteristic curves and evaluated at $V_{GS}$ = −3 V and $V_{DS}$ = 10 V. Closed (open) symbols denote measurements on devices with gate length $L_G$ = 220–400 nm (1 μm).

thickness $d_{UID}$ larger than 200 nm either vanishes or is insignificant as compared to self-heating effects, which can lead to apparently negative output conductance. On a given sample we do not observe any difference in output conductance between devices with $L_{DS}$ = 3 μm compared with those with $L_{DS}$ = 5 μm. In addition we do not observe a significant difference in the output conductance of Samples E and G, for which $L_G$ = 1 μm, compared to Sample A, which has the same $d_{UID}$ but shorter gate length ($L_G$ = 240 nm). The output conductance of each of these three samples is within the range of experimental uncertainty of the other two. This suggests that short channel effects associated with low $L_G$-to-barrier thickness ratios do not significantly contribute to the output conductance of devices on these samples [17]. We speculate that the observed output conductance arises from a parallel conducting path which passes vertically through the depleted UID buffer and laterally along the Be-doped layer. As the UID buffer is made thinner its contribution to the total series resistance decreased, providing an increasingly significant leakage pathway, especially as the AlGaN/GaN channel is depleted.

Likewise, inter-device isolation current measurements provide an indication of parallel conduction in the buffer layer underlying the 2DEG. We measured isolation currents at 1-V bias steps in the range from −100 to +100 V across concentric ohmic contacts separated by a 16-μm wide annulus in which the 2DEG was removed by the 500-Å ICP mesa etch. The diameter of the inner electrode was 100 μm. Further details of this measurement are given elsewhere [15,18]. All samples exhibited excellent isolation characteristics (<1 μA at 5 V bias). Nevertheless, we observed a trend toward increased leakage as $d_{UID}$ decreased (Fig. 5), consistent with parallel conduction in the Be-doped layer. Further evidence for this interpretation comes from Sample A, which underwent a second 500-Å mesa etch. While the first mesa etch removed the 250-Å AlGaN barrier and half of the 50 nm UID buffer, the second removed the rest of the UID buffer and the first 25 nm of the Be-doped layer. Isolation currents were measured after the first and second mesa etches, and the reduction in current after the second etch compared to the first was only 5–10%, indicating that at least 80% of the current passes vertically through the UID layer and into the Be-doped layer. Thus the observed decrease in isolation current with increasing UID buffer thickness argues that there is minimal lateral conduction in the UID GaN layer in these samples. However, we anticipate that significantly increasing $d_{UID}$ beyond 500 nm would again lead to large leakage currents due to uncompensated carriers arising from the aforementioned background concentration of oxygen in the UID layer.

Gate lag measurements were performed on five of the seven samples in order to determine the effect of $d_{UID}$ on dispersion. This measurement is very similar to that described by Binari et al. [19] and Edwards et al. [20] except for a load resistor placed in series with the device under test. The load resistance is chosen to permit $V_{DS}$ to vary from a maximum of 20 V when the device is pinched off ($V_{GS}$ = −8 V) to the knee voltage when $V_{GS}$ = 0, and it serves to limit the maximum instantaneous power dissipated in the device to ~25% of what it would otherwise be. The gate pulse duration is 500 ns. Gate lag ratios on unpassivated devices varied monotonically from 0.07 for $d_{UID}$ = 50 nm to 0.5 for $d_{UID}$ = 500 nm. Following the deposition of a 1000-Å $SiN_x$ passivation layer the gate lag still

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increased monotonically, from 0.44 to 0.84, as $d_{UID}$ increased from 50 nm to 200 nm. Typical post-passivation gate lag ratios of HEMTs with $d_{UID}$ = 500 nm are ~0.9. Since $SiN_x$ effectively passivates surface traps, these results suggest that trapping effects in these heterostructures are predominantly associated with surface traps when $d_{UID} \geqslant 200$ nm whereas both surface and buffer trapping contribute to dispersion when $d_{UID} < 200$. The power output characteristics of these devices were measured at a frequency of 4 GHz. The power output density increased monotonically over the range of UID layer thicknesses from 50 to 200 nm, consistent with the gate lag results. Thus we conclude that the optimal range of UID buffer thicknesses is between 200 nm and 500 nm.

## 4. Conclusion

In conclusion, we have grown seven AlGaN/GaN heterostructures by rf-plasma MBE on free-standing, HVPE-grown GaN substrates. The thickness of the UID GaN buffer layer between the AlGaN barrier and the Be-doped GaN layer was varied from 50 nm to 500 nm. Process control monitors, including Hall and inter-device isolation patterns, and HEMTs were defined on all samples using standard lithography. Hall mobility and sheet density decreased, and Hall sheet resistance increased, as the thickness of the UID GaN buffer decreased. The improvement of Hall properties with increasing buffer thickness was greatest for $d_{UID} < 200$ nm, and only minor improvements were observed when $d_{UID}$ increased further to 500 nm. Likewise, as $d_{UID}$ decreased below 200 nm, output conductance increased significantly. We observed no evidence to indicate that output conductance in these devices depended on gate length, indicating short channel effects did not significantly contribute to the output conductance. We tentatively attribute this increase in output conductance with diminishing $d_{UID}$ to the reduction of the series resistance vertically through the depleted UID GaN buffer to a more conductive Be-doped layer. This interpretation is supported by inter-device isolation current measurements, which also exhibit an increase in leakage current as $d_{UID}$ diminishes. Gate lag measurements after $SiN_x$ passivation suggest that the microwave performance of devices with $d_{UID} < 200$ nm are limited by buffer traps. On the basis of this investigation we conclude that an optimized buffer needs to include Be-doped GaN isolation layers in MBE-grown AlGaN/GaN HEMTs and must be separated from the 2DEG by 200 nm to 500 nm.

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